User's Guide

M0116SD-161SDBR1-1

VFM- RoHS Compliant

(Vacuum Fluorescent Display Module)

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1. SCOPE

This specification applies to VFD module (Model No: M0116SD-161SDBR1-1) .

2. FEATURES

2.1 LCD compatible interface and mounting holes.
(This VFD module is capable to communicate some different type of bus systems such as i80 (Intel) or M68 (Motorola), 8-bit or 4-bit parallel data.), or a synchronous serial interface.

2.2 High quality of display and luminance.

2.3 Compact and light-weight unit by using new VFD technology and flat packed one-chip controller.

2.4 +5V single power supply.

2.5 Luminance adjustment available by software (4 levels).

2.6 8 user definable fonts available (CG-RAM font).

2.7 ASCII and Japanese Katakana characters (CG-ROM font).

3. GENERAL DESCRIPTIONS

3.1 This specification becomes effective after being approved by the purchaser.

3.2 When any conflict is found in the specification appropriate action shall be taken upon agreement of both parties.

3.3 The expected necessary service parts should be arranged by the customer before the completion of production.

4. PRODUCT SPECIFICATIONS

4.1 Type

Table-1

Type	M0116SD-161SDBR1-1
Digit Format	5×8Dot Matrix with Cursor

4.2 Outer Dimensions, Weight (See Fig-7 on Page 6/20 for details)

Table-2

Parameter		Specification	Unit
Outer Dimensions	Width	80.0±1.0	mm
	Height	36.0±1.0	mm
	Thickness	9.35 Max	mm

4.3 Specification of the Display Panel (See Fig-9 on Page 7/20 for details) Table-3

Parameter	Symbol	Specification	Unit
Display size	W*h	51.5*5.29	mm
Number of digit	W*H	16 digits*1 line	
Character Size	W*H	2.8*5.29	mm
Character Pitch	W*H	1.27*5.29	mm
Dot Size	W*H	0.28*0.53	mm
Display color	W*H	Green (X=0.250,Y=0.439)	

4.4 Environment Conditions Table-4

Parameter	Symbol	Min	Max	Unit
Operating temperature	Topr	-40	+80	° C
Storage temperature	Tstg	-50	+95	° C
Humidity(operating)	Topr	0	85	%
Humidity(non-operating)	Hstg	0	90	%
Vibration(5-55hz)	-	-	4	G
shock	-	-	40	G

4.5 Absolute Maximum Ratings Table-5

parameter	Symbol	Min	Max	Unit
Supply voltage	Vic	-0.5	6.0	Vdc
Input signal voltage	Vis	-0.5	Vcc+0.5	Vdc

4.6 Recommend Operating Conditions Table-6

Parameter	Symbol	Min	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	Vdc
Input signal voltage	Vis	0	-	Vcc	Vdc
Operating temperature	Topr	-20	+50	+70	° C

4.7 DC Characteristics (Ta=+25 ℃, Vcc=+5.0Vdc) Table-7

Parameter		Symbol	Min.	Typ.	Max	Unit
Supply current ※)		Icc	-	90.5	108	mA
Logical input voltage	H	Vih	0.7*Vcc			
	L	vil	-			
"H" level input current	Vcc	Iih	20			
Luminance		L	102 (350)	200 (680)	-	Ft-l cd/m²

※) Icc shows the current when all dots are turned on. The surge current can be approx.3 times the specified supply current at power on. However, the exact peak surge current amplitude and duration are dependent on the characteristics of the host power supply.

4.8 Timing Chart and AC Characteristics

4.8.1 Power-on Reset and /or REST Signal Timing

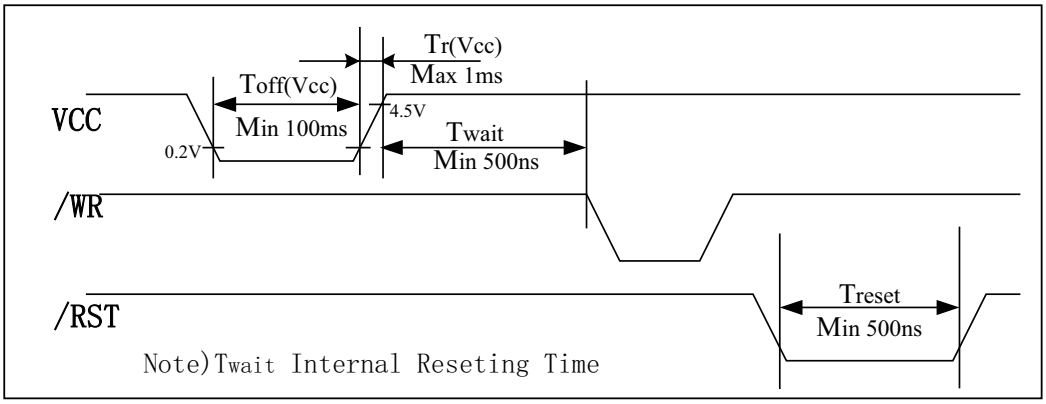


Fig-1 Power-on Reset and RESET signal Timing

4.8.2 I80 type CPU bus write in Timing

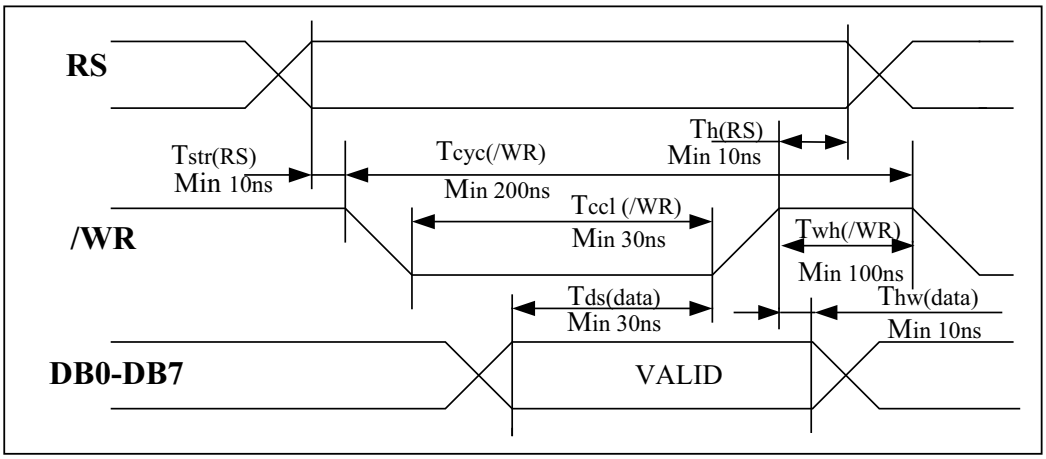


Fig –2 Data write-in Timing Diagram

4.8.3 i80 type CPU bus read-out Timing

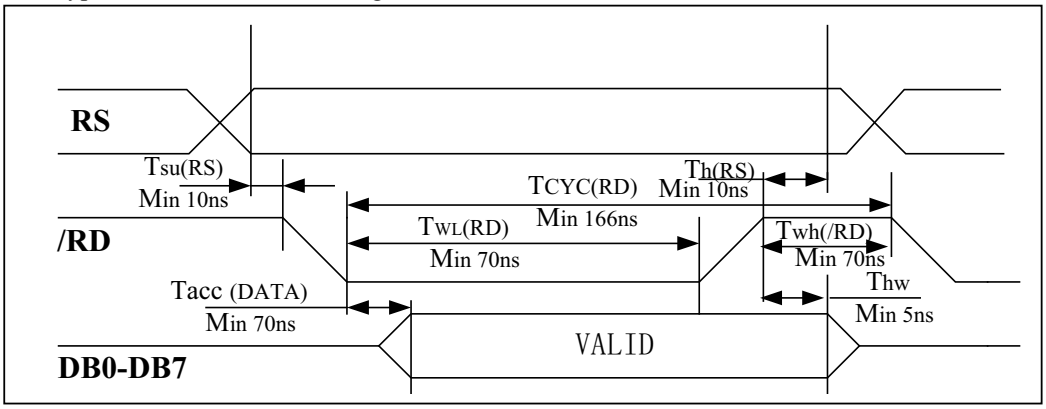


Fig-3 Dada Read-out Timing Diagram (i80 bus interface)

4.8.4 M68 type CPU bus write in timing

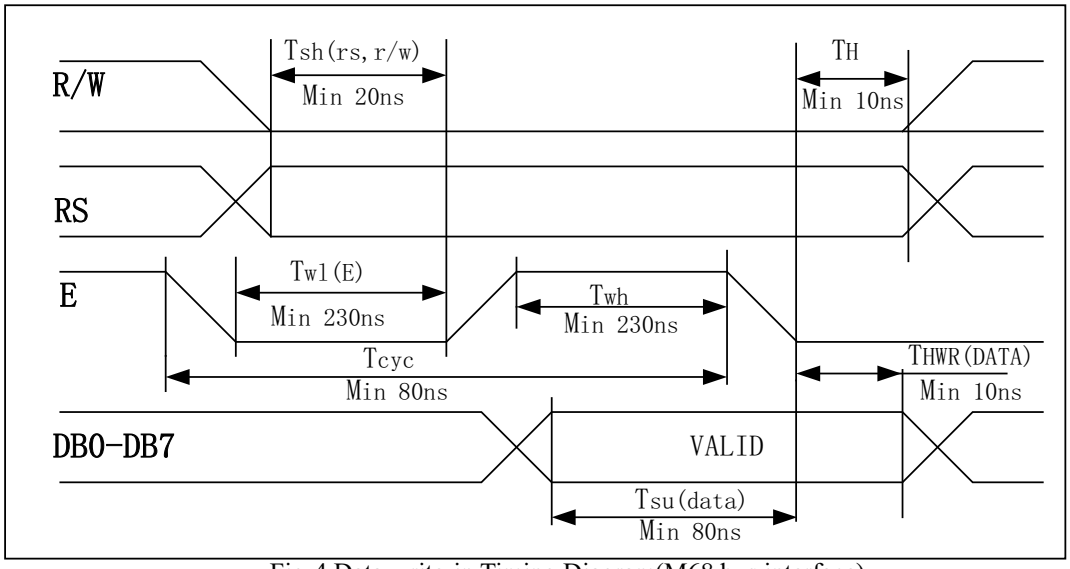


Fig-4 Data write-in Timing Diagram(M68 bus interface)

4.8.5 M68 type CPU bus read-out Timing

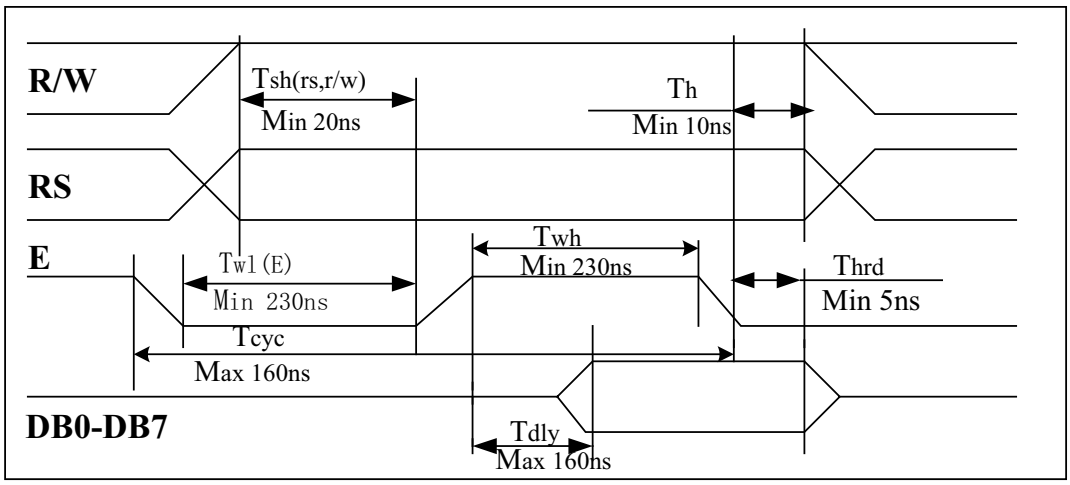


Fig-5 Data read-out Timing Diagram (M68)

4.8.6 Synchonous Serial Interface Timing

Item	Symbol	Min.	Max.	Unit
STB setup time	t_{STBS}	100	-	ns
STB hold time	t_{STBH}	500	-	ns
Input signal fall time	t_f	-	15	ns
Input signal rise time	t_r	-	15	ns
STB pulse width high	t_{WSTB}	500	-	ns
SCK pulse width high	t_{SCKH}	200	-	ns
SCK pulse width low	t_{SCKL}	200	-	ns
SI data setup time	t_{DSs}	100	-	ns
SI data hold time	t_{DHs}	100	-	ns
SCK cycle time	t_{CYCSCK}	500	-	ns
SCK wait time between bytes	t_{WAIT}	1	-	us
SO data delay time	t_{DDs}	-	150	ns
SO data hold time	t_{DHRs}	5	-	ns

Note: All timing is specified using 20% and 80% of V_{CC} as the reference points.

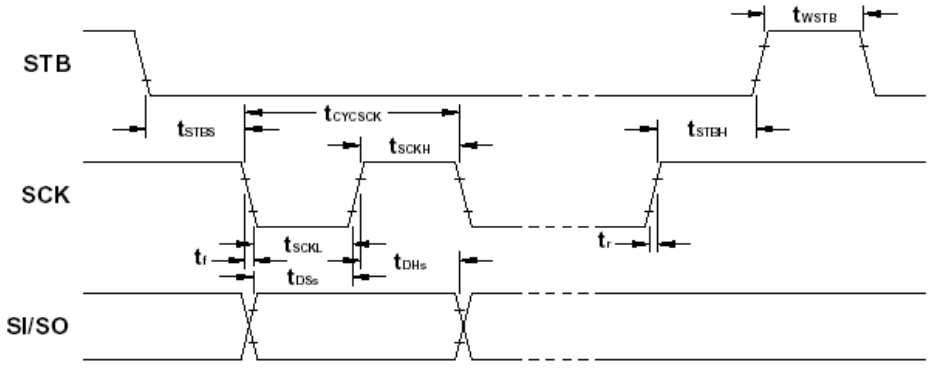


Figure 6. Synchronous Serial Interface Write Cycle Timing

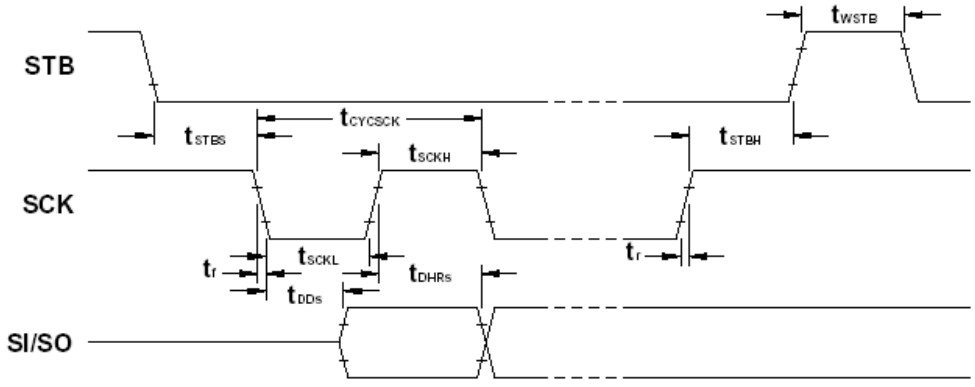


Figure 7. Synchronous Serial Interface Read Cycle Timing

4.9 SYSTEM BLOCK DIAGRAM

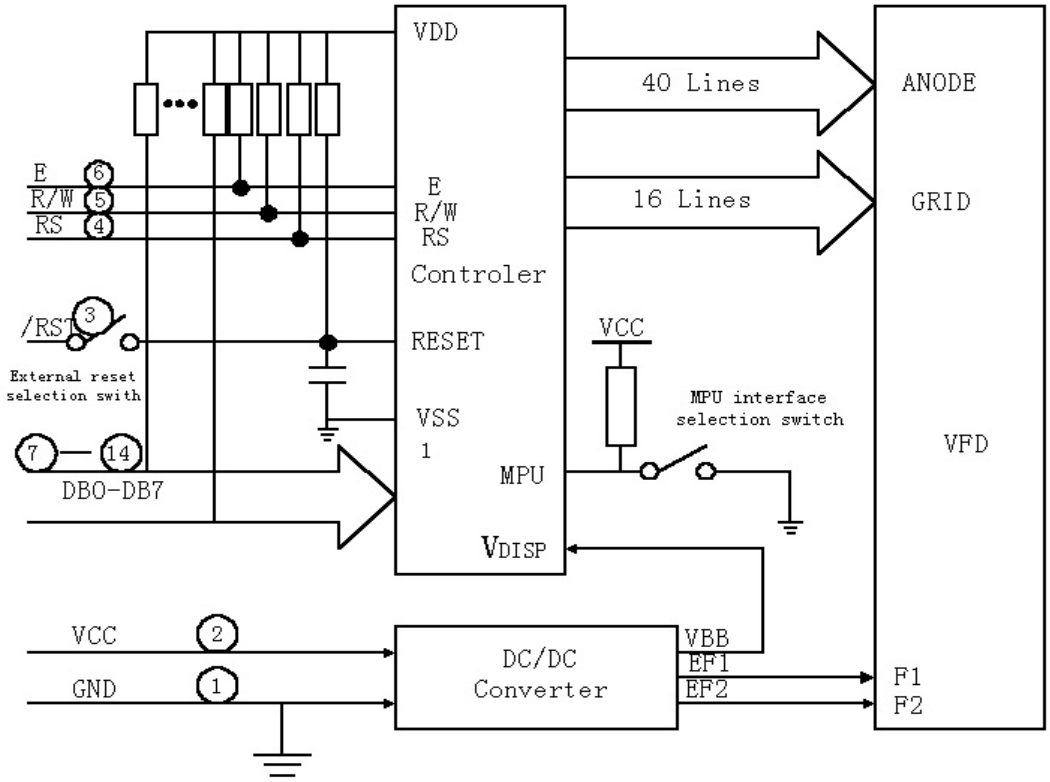


Fig-6 System Block Diagram of this VFD Module

4.10 Outer Dimensions

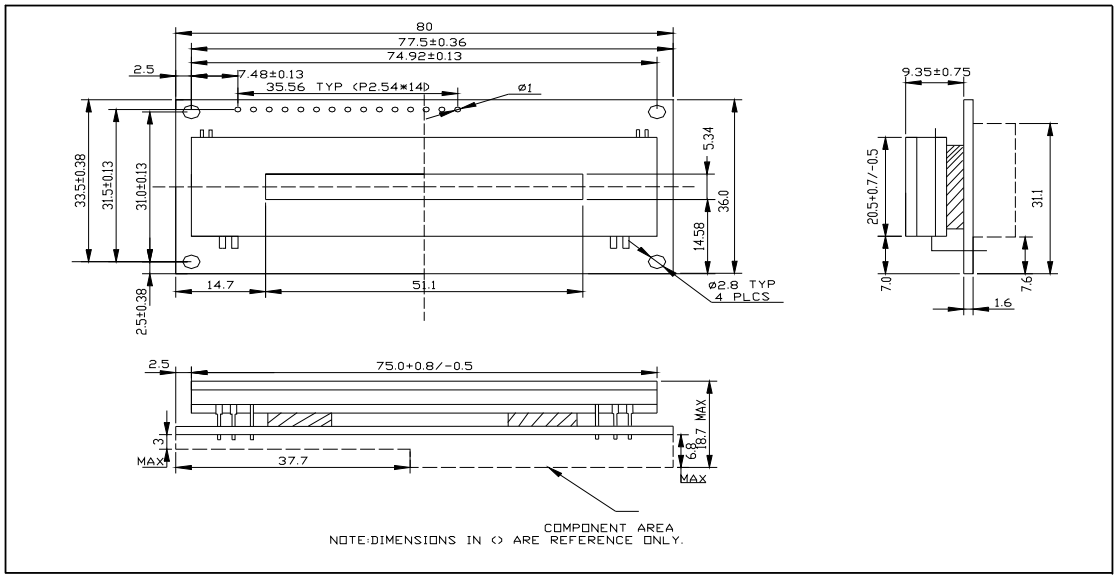


Fig-7 Outer dimensions

4.11 Connecter Through Hole Location

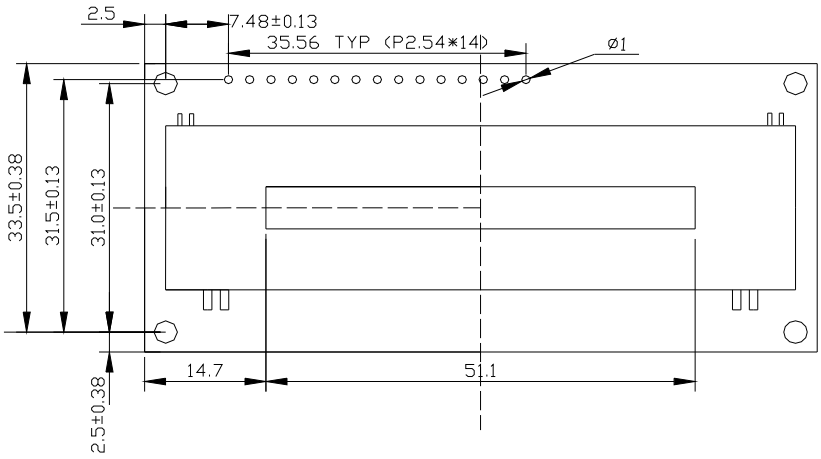
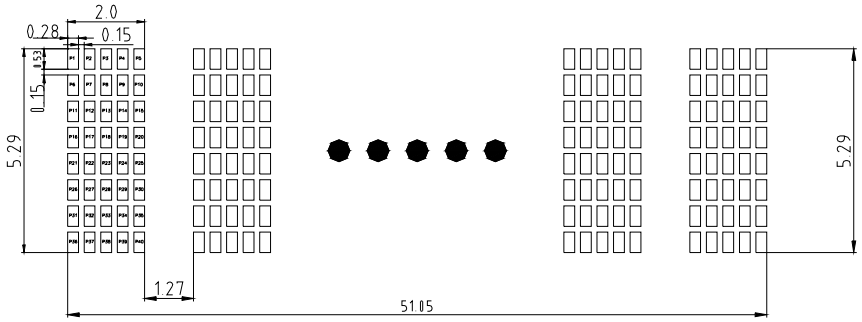


Fig-8 15-pin Through Hole Dimensions

4.12 Pattern Details



5.FUNCTION DESCRIPTIONS

5.1 Registers in VFD Controller

The VFD controller has two 8-bit registers, an instruction register (IR) and a data register (DR). IR stores instruction codes, such as display clear and cursor shift, and address information for DD-RAM and CG-RAM The IR can only be written from the host MPU.DR temporarily stores data to be written into DD-RAM or CG-RAM and temporarily stores data to be read from DD-RAM or CG-RAM. Data written into the DR from the MPU is automatically written into DD-RAM or CG-RAM by an internal operation. The DR is also used for data storage when reading data from DD-RAM or CG-RAM. When address information is written into the IR , data is read and then stored into the DR from DD-RAM or CG-RAM by internal operation. Data transfer between MPU is then completed when the MPU reads the DR. After the read, data in DD-RAM or CG-RAM at the next address is send to the DR for the next read from the MPU. By the register selector (RS) signal. These two registers can be selected (See Table-8).

Table-8 Register Selection

RS	M68	i80		Operation
	R/W	/RD	/WR	
0	0	1	0	IR write as an internal operation (display clear, ect.)
0	1	0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	1	0	DR write as an internal operation (DR to DD-RAM or CG-RAM)
1	1	0	1	DR read as an internal operation (DD-RAM or CG-RAM to DR)

5.1.1 Busy Flag (BF)

When the busy flag is 1, the controller is in the internal operation mode, and the next instruction will not be accepted. When RS =0 and R/W=1 (Table-8), the busy flag is output to DB7.

The next instruction must be written after ensuring that the busy flag is 0.

5.1.2 Address Counter (ACC)

The address counter (ACC) assigns addresses to both DD-RAM and CG-RAM. When an address of an instruction is written into the IR, the address information is sent from the IR to the ACC. Selection of either DD-RAM or CG-RAM is also determined concurrently by the instruction. After writing into (reading from) DD-RAM or CG-RAM, the ACC is automatically incremented by 1 (decremented by 1). The ACC contents are then output to Db0 to Db6 when RS =0 and R/W=1 (See Table-8).

5.1.3 Display Data RAM (DD-RAM)

Display data RAM (DD-RAM) stores display data represented in 8-bit character codes.

The area in DD-RAM that is not used for display can be used as general data RAM.

See Table-9 for the relationships between DD-RAM addresses and positions on the VFD

Table-9 Relation between Digit Position and DD-RAM data

	Left End	2nd Column	3rd column	- - - - - - - - - - -	15th Column	Right End
1st Row	00H	01H	02H	- - - - - - - - - - - -	0EH	0FH

5.1.4 Character Generator ROM (CG-ROM)

The character generator ROM (CG-ROM) generates character patterns of 5x8 dots from 8-bit character codes (table-10). It can generate 240 kinds of 5x8 dots character patterns.

The character fonts are shown on the following page. The character codes 00H to 0FH are allocated to the CG-RAM.

5.1.5 Character Generator RAM (CG-RAM)

In the character generator RAM (CG-RAM), the user can rewrite character patterns by program.

For 5×8 dots and cursor, eight character patterns can be written. Write into DD-RAM the character codes at the addresses shown as the left column of Table-10 to show the character patterns stored in CG-RAM.

See Table-11 for the relationship between CG-RAM addresses and data and display patterns and refer to Fig-10 for dot assignment of VFD.

Areas that are not used for display can be used as general data RAM

1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20
21	22	23	24	25
26	27	28	29	30
31	32	33	34	35
36	37	38	39	40

Table-10 Characters Font Table (CG-ROM)and CG-RAM codes

Upper bits / Lower bits		DB7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		DB6	0	0	0	0	1	1	1	1	0	0	0	1	1	0	1	1
		DB5	0	0	0	1	1	0	0	1	1	0	0	1	0	1	1	1
		DB4	0	1	0	1	0	0	1	0	1	0	1	0	0	1	0	1
DB0 DB1 DB2 DB3			0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
0 0 0 0	**0**	CG-RAM (1)				0	@	P	`	p	Ä	Æ		—	タ	ミ	α	p
0 0 0 1	**1**	CG-RAM (2)		!	1	A	Q	a	q	ä	æ	。	ア	チ	ム	ä	q
0 0 1 0	**2**	CG-RAM (3)		"	2	B	R	b	r	Å	£	「	イ	ツ	メ	ß	Θ
0 0 1 1	**3**	CG-RAM (4)		#	3	C	S	c	s	á	Ñ	」	ウ	テ	モ	ε	∞
0 1 0 0	**4**	CG-RAM (5)		$	4	D	T	d	t	à	●	、	エ	ト	ヤ	μ	Ω
0 1 0 1	**5**	CG-RAM (6)		%	5	E	U	e	u	E	o	・	オ	ナ	ユ	σ	ü
0 1 1 0	**6**	CG-RAM (7)		&	6	F	V	f	v	ö	♦	ヲ	カ	ニ	ヨ	ρ	Σ
0 1 1 1	**7**	CG-RAM (8)		'	7	G	W	g	w	ö	◇	ァ	キ	ヌ	ラ	g	π
1 0 0 0	**8**	CG-RAM (1)		(	8	H	X	h	x	ø	¡	ィ	ク	ネ	リ	ɾ	x̄
1 0 0 1	**9**	CG-RAM (2)		)	9	I	Y	i	y	ø	Ç	ゥ	ケ	ノ	ル	'	y
1 0 1 0	**A**	CG-RAM (3)		*	:	J	Z	j	z	ü	Δ	ェ	コ	ハ	レ	j	∓
1 0 1 1	**B**	CG-RAM (4)		+	;	K	[	k	{	ü	¿	ォ	サ	ヒ	ロ	ˣ	Ħ
1 1 0 0	**C**	CG-RAM (5)		,	<	L	¥	l	|	\	¿	ャ	シ	フ	ワ	¢	円
1 1 0 1	**D**	CG-RAM (6)		-	=	M	]	m	}	≠	↵	ュ	ス	ヘ	ン	ŧ	÷
1 1 1 0	**E**	CG-RAM (7)		.	>	N	^	n	→	∿	↑	ョ	セ	ホ	゛	ñ	
1 1 1 1	**F**	CG-RAM (8)		/	?	O	_	o	←	§	↓	ッ	ソ	マ	゜	ö	

Table-11 Relationship between CG-RAM address, Character Codes (DD-RAM) AND 5*7 (whit Cursor) Dot Character Patterns (CG-RAM)

Character Codes (DD-RAM DATA)								CG-RAM ADDRESS						Character Patterns (CG-RAM data)								
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	×	0	0	0	0	0	0	0	0	0	×	×	×	1	2	3	4	5	Character Pattern(0)
											0	0	1	×	×	×	6	7	8	9	10	
											0	1	0	×	×	×	11	12	13	14	15	
											0	1	1	×	×	×	16	17	18	19	20	
											1	0	0	×	×	×	21	22	23	24	25	
											1	0	1	×	×	×	26	27	28	29	30	
											1	1	0	×	×	×	31	32	33	34	35	
											1	1	1	×	×	×	36	×	×	×	×	Cursor
0	0	0	0	×	0	0	1	0	0	1	0	0	0	×	×	×	1	2	3	4	5	Character Pattern (1)
											0	0	1	×	×	×	6	7	8	9	10	
											0	1	0	×	×	×	11	12	13	14	15	
											0	1	1	×	×	×	16	17	18	19	20	
											1	0	0	×	×	×	21	22	23	24	25	
											1	0	1	×	×	×	26	27	28	29	30	
											1	1	0	×	×	×	31	32	33	34	35	
											1	1	1	×	×	×	36	×	×	×	×	Cursor
0	0	0	0	×	1	1	1	1	1	1	0	0	0	×	×	×	1	2	3	4	5	Character Pattern(7)
											0	0	1	×	×	×	6	7	8	9	10	
																						Cursor

Notes: 1. Character code bits 0 to2 correspond to CG-RAM address bits 3 to 5 (3 bits 8 types).

2. CG-RAM address bits 0 to 2 designate the character the patter line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line If bit 4of the 8th line data is 1.1 bit will light up the cursor regardless of the cursor presence

3. Character pattern row positions correspond to CG-RAM data bits 0 to 4 (bit 4 being at the left)

4. As show Table-11 CG-RAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect , the display example above can be selected by either character code 00H or 08H

5. 1 for CG-ram data corresponds display selection and 0 to non-selection."×" Indicates non-effect.

5.2 Interfacing to the MPU

This VFD module can interface in either two 4-bir operations or one 8-bit operation, thus allowing interfacing with 4-bit or 8-bit MPUs.

※ For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer. When to use 4-bit parallel data transfer, DB0 to DB3 keep “H”or “L”. The data transfer between the VFD module and the MPU is completed after the 4-bit data has been transferred before the four low order bits (for 8-bit operation. DB0 to DB3).

The busy flag (BF) are performed before transferring the higher 4 bits. BF checks are not required before transferring the lower 4 bits.

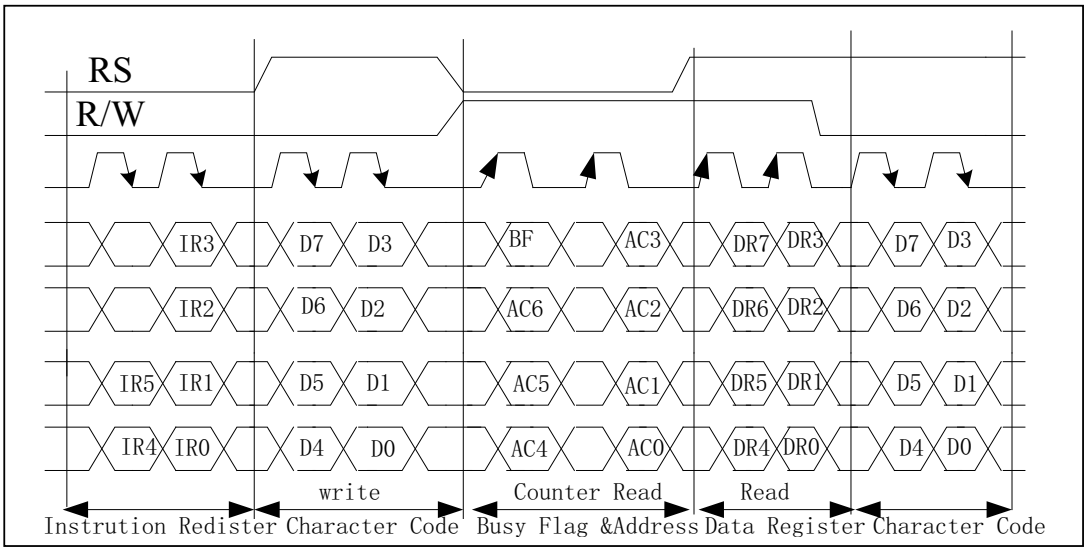


Fig 4-biti transfer Example (M68)

※For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.

5.3 Reset Function

5.3.1 Power-on reset

An internal reset circuit automatically initializes the module when the power is turn on.

The following instructions are executed during the initialization.

1) Display clear
   Fill the DD-RAM with 20H (Space Code)
2) Set the address counter to 00H
   Set the address counter (ACC) to point DD-RAM.

3) Display on/off control:
   D=0; Display off
   B=0; Blinking off
   C=0; Cursor off
4) Entry mode set:
   L/D=1; Increment by 1
   S=0; No shift
5) Function set
   IF=1; 8-bit interface data
   BR0=BR1=0; Brightness=100%
   N=1; 2-line display
6) CPU interface type
   When JP0=Open; M68 type (Factory Setting)
   When JP0=Short; i80 type

5.3.2 External

In order to use this function, a user must connect the soldering pad "JP1". When the soldering pad "JP1" is open-circuited, this function is not valid and when it is short-circuited, the third hole (pin #3) is used for external reset input. If low level signal longer than 500ns is input into the hole, reset function being same as power on reset is executed.

5.4 Soldering Land Function

Some soldering lands are prepared on the rear side of PCB, to set operating mode of the display module. A soldering iron is required to short soldering lands.

Table-12 Soldering Land OPEN/SHORT Combination Table

Mode	JP2	JP3	JP4	JP5	JP6	JP7
Parallel (Motorola)	(Note 1)	open	shorted	open	shorted	open
Parallel (Intel)	(Note 1)	open	shorted	open	open	shorted
Serial	open	shorted	open	shorted	shorted	open

Note 1: JP2 shorted (open) enables (disables) external reset mode.

6. INSTRUCTIONS

6.1 Outline

Only the instruction register (IR) and data register (DR) of the VFD controller can be controlled by the user's MPU. Before starting the internal operation of the controller, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the controller is determined by signals sent from the MPU. These signals, which include register selection signal (RS), read/write signal (R/W), and the data bus (DB0 to DB7), make up the controller instructions (See Table-13). There are four categories of instructions that:

- designate controller functions, such as display format, data length, ect.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally instructions that perform data transfer with interval RAM are used the most.

However, auto-increment by 1 (or auto-decrement by 1) of internal RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed. Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note: Be sure the controller is not in the busy state (BF=0) before sending an instruction from the MPU to the nodule. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself.
Refer to Table-13 for the list of each instruction execution time.

Table –13 Instruction Set

Instruction	CODE										Description
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Display clear	0	0	0	0	0	0	0	0	0	1	Clear all display and sets DD-ram address 0 in address counter
Cursor Home	0	0	0	0	0	0	0		1	×	Sets DDRAM address 0 in ACC. Also returns the display being shifted to the original position DD RAM contents remain unchanged
Entry Mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor direction and specifies display shift. These operations are during WR/RD data
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets all display ON/OFF(D),cursor ON/OFF(C),cursor blink of character position(B)
Cursor or display Shift	0	0	0	0	0	1	S/C	R/L	×	×	Shifts display or cursor, keeping DD-RAM contents.
Function set	0	0	0	0	1	IF	N	×	BR1	BR0	Sets data length (IF), number of display lines (N), Set brightness level (BR1, BR0)
CGRAM address Setting	0	0	0	1	ACG						Sets the CG-RAM address.
DDRAM Address setting	0	0	1	ADD							Sets the DD-RAM address.
Busy flag & address setting	0	1	BF	ACC							Read busy flag (BF) and address counter (ACC).

Data write to CG or DDRAM	1	0	Data writing	Writes data into CG-RAM or DD-RAM
Data Read from CG or DDRAM	1	1	Data reading	Read data from CG-RAM or DD-RAM
※NOTE	I/D=1: Increment I/D=0: Decrement S=1: Display shift enabled S=0: Cursor shift enabled S/C=1: Display shift S/C=0: Cursor move R/L=1: Shift to the right R/L=0: Shift to the left IF=1: 8bits IF=0: 4bits N=1: 2 Lines display N=0:1 Lines display BR1, BR0= 00: 100% 01: 75% 10: 50% 11: 25% BF=1:Busy (Internally operating). BF=0:Not busy (Instruction acceptable) .: Don't care			[Abbreviation] DD-RAM: Display Data RAM CG-RAM: Character Generater RAM ACG: CG-RAM Address ADD: DD-RAM Address ACC: Address Counter

6.2 Instruction Description

6.2.1 Display Clear

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1

RS=0, R/W=0

This instructions

(1) Fills all locations in the display data RAM (DD-RAM) with 20H (Blank-character).

(2) Clears the contents of the address counter (ACC) to 00H.

(3) Sets the display for zero character shift (returns original position).

(4) Sets the address counter(ACC) to point to the DD-RAM.

(5) If the cursor is displayed, moves the cursor to the left most character in the top line (upper line).

(6) Sets the address counter (ACC) to increment on the each access of DD-RAM or CG-RAM.

6.2.2 Cursor Home

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	×

RS=0, R/W=0 02H to 03H ×: Don't care

This instruction

(1) Clears the contents of the address counter (ACC) to 00H.

(2) Sets the address counter (ACC) to point to the DD-RAM.

(3) Sets the display for zero character shift (returns original position).

(4) If the cursor is displayed, moves the left most character in the top line (upper line).

6.2.3 Entry Mode Set

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	I/D	S

RS=0, R/W=0 04H to 07H

The I/D bit selects the way in which the contents of the address counter (ACC) are modified after every access to DD-RAM or CG-RAM.

I/D=1: The address counter (ACC) is incremented.

I/D=0: The address counter (ACC) is decremented.

The S bit enable display shift, instead of cursor shift , after each write or read to the DD-RAM.

S=1: Display shift enabled.

S=0: Cursor shift enabled.

The direction in which the display is shifted is opposite in sense to that of the cursor.

For example, if S=0 and I/D=1, the cursor would shift one character to the right after a MPU writes to DD-RAM. However if S=1 and I/D=1, the display would shift one character to the left and the cursor would maintain its position on panel.

The cursor will already be shifted in the direction selected by I/D during reads of the DD-RAM, irrespective of the value of S. Similarly reading and writing the CG-RAM always shift the cursor.

Also both lines are shifted simultaneously.

Table-14 Cursor move and Display shift by the "Entry Mode Set"

I/D	S	After writing DD-RAM data	After reading DD-RAM data
0	0	The cursor moves one character to the left.	The cursor moves one character to the left.
1	0	The cursor moves one character to the right.	The cursor moves one character to the right.
0	1	The display shifts one character to the right without cursor's move.	The cursor moves one character to the left.
1	1	The display shifts one character to the left without cursor's move.	The cursor moves one character to the right.

6.2.4 Display ON/OFF

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	D	C	B

RS=0, R/W=0 08H to 0FH

×: Don't care

This instruction controls various features of the display.

D=1: Display on , D=0: Display off.

C=1: Cursor on C=0: Cursor off.

B=1: Blinking on B=0: blinking off.

(Blinking is achieved by alternating between a normal and all on display of a character.
The cursor' blink with a frequency of about 1.0 Hz and DUTY 50%)

6.2.5 Cursor/Display Shift

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	S/C	R/L	0	0

RS=0, R/W=0 10H to 1FH

×: Don't care

This instruction shifts the display and/or moves the cursor on character to the left or right, without reading or writing DD-RAM.

The S/C bit selects movement of the cursor or movement of both the cursor and the display.

S/C=1: Shift both cursor and display

S/C=0: Shift cursor only

The R/L bit selects left ward or right ward movement of the display and/or cursor.

R/L=1: Shift one character right

R/L=0: Shift one character left

Table-15 Cursor/Display shift

S/C	R/L	Cursor shift	Display shift
0	0	Move one character to the left	No shift
0	1	Move one character to the right	No shift
1	0	Shift one character to the left with display	Shift one character to the left
1	1	Shift one character to the right with display	Shift one character to the right

6.2.6.Function Set

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	IF	N	×	BR1	BR2

RS=0, R/W=0 20H to 3FH

×: Don't care

This instruction sets width of data bus line.(when to use parallel interface. IM=1). The number of display line and brightness control.

This instruction initializes the system, and must be the first instruction executed after power-on.

The IF bit selects between an 8-bit or 4-bit bus width interface.

IF=1: 8-bit CPU interface using DB7 to DB0

IF=0: 4-bit CPU interface using DB7 to DB4

The N bit selects between 1-line or 2-line display.

N=1: Select 2 line display (Using anode output A1 to A80)

N=0: Select 1 line display (Using anode output A1 to A40. A41 to A80 fixed Low level.)

BR1, BR0 flag is control to brightness of VFD to modulate pulse width of Anode output as follows.

BR1	BR0	Brightness
0	0	100%
0	1	75%
1	0	50%
1	1	25%

6.2.7 Set CG-RAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	ACG					

RS=0, R/W=0 40H to 7FH

×: Don't care

This instruction

(1) Load a new 60bit address into the address counter (ACC).

(2) Sets the address counter (ACC) to address CG-RAM.

Once "Set CG-RAM Address" has been executed, the contents of the address counter (ACC) will be automatically modified after every access of CG-RAM, as determined by the "Entry Mode Set" instruction.

The active width of the address counter (ACC), when it is addressing CG-RAM, is 6-bit, so the counter will wrap around to 00H from 3FH if more than 64 bytes of data are written to CG-RAM

6.2.8 Set DD-RAM Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	ADD						

RS=0, R/W=0 80H to A7H (1-Line)

C0H to E7h (2-line)

×: Don't care

This instruction

(1) Loads a new 7-bit address into the address counter (ACC).

(2) Sets the address counter (ACC) to point to the DD-RAM.

Once the “Set DD-RAM Address” instruction has been executed, the contents of the address counter (ACC) will be automatically modified after each access of DD-RAM, as selected by the “Entry Mode Set” instruction.

Table-16 Valid DD-RAM address Ranges

	Number of Character	Address Range
1st line	40	00H to 27H
2nd line	40	40H to 67H

6.2.9 Read Busy Flag and Address

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
BF	ACC						

RS=0, R/W=1

Read busy flag and address reads the flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress.

BF=1: busy state

BF=0: ready for next instruction, command receivable.

The next instruction will not be accepted until BF is reset to 0.Check the BF status before the next write operation. At the same time, the value of the address counter (ACC) in binary AAAAAAA is read out. This address counter (ACC) is used by both CG-RAM and DD-RAM address and its value is determined by the previous instruction. The address counter are the same as for instructions set CG-RAM address and set DD-RAM address.

6.2.10 Write Data to CG or DD-RAM

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Data Read							

RS=1, R/W=0

This instruction writes 8-bit binary data (DB7 to DB0) from CG-RAM or DD-RAM.

The previous designation determines whether CG-RAM or DD-RAM is to be read.

Before entering this read instruction, either CG-RAM or DD-RAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor shift instruction (when reading out DD-RAM).

The operation of the cursor shift instruction is the same as the set DD-RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1.

Note: The address counter (ACC) is automatically incremented or decremented by 1 after the write instructions to CG-RAM or DD-RAM are executed. The RAM data selected by the ACC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DD-RAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.

7. 0 PERATING RECOMMENDATIONS

7.1 Avoid applying excessive shock or vibration beyond the specification for the VFD module.

7.2 Since VFDs are made of glass material, careful handling is required.
i.e. Direct impact with hard material to the glass surface (especially exhaust tip) may crack the glass.

7.3 When mounting the VFD module to your system, leave a slight gap between the VFD glass and your front panel. The module should be mounted without stress to avoid flexing of the PCB.

7.4 Avoid plugging or unplugging the interface connection with the power on, otherwise it may cause the severe damage to input circuitry.

7.5 Slow starting power supply may cause non-operation because one chip Mico won't be reset.

7.6 Exceeding any of maximum ratings may cause the permanent damage.

7.7 Since the VFD modules contain high voltage source, careful handing is required during powered on.

7.8 When the power is turned off, the capacitor dose not discharge immediately.
The high voltage applied to the VFD must not contact to the ICs. And the short-circuit of mounted components on PCB within 30 times the specified current consumption when the power is turned on.

7.9 The power supply must be capable of providing at least 3 times the rated current, because the surge current can be more than 3 times the specified current consumption when the power is turned on.

7.10 Avoid using the module where excessive noise interference is expected. Noise may affects the Interface signal and causes improper operation. And it is important to keep the length of the interface cable less than 50cm.

7.11 Since all VFD modules contain C-MOS ICs, anti-static handing procedures are always required.

NOTE: Newhaven Display reserves the right to change or modify this spec or design without notice in order to improve the quality or design of this product.

8.0 CONNECTOR INTERFACE

Pin No.	Serial	Parallel (Intel)	Parallel (Motorola)	Pin No.	Serial	Parallel (Intel)	Parallel (Motorola)
1	GND	GND	GND	2	V_{CC}	V_{CC}	V_{CC}
3	SI/SO	NC or RST/	NC or RST/	4	STB	RS	RS
5	NC	WR/	R/W	6	SCK	RD/	E
7	NC	DB0	DB0	8	NC	DB1	DB1
9	NC	DB2	DB2	10	NC	DB3	DB3
11	NC	DB4	DB4	12	NC	DB5	DB5
13	NC	DB6	DB6	14	NC	DB7	DB7

NC = No Connection